REMARKS

Claims 1-19 and 33-45 are pending in this application. Claims 20-32 have been finally withdrawn from consideration and so have been cancelled. Claims 33-45 have been added.

The Restriction Requirement

The Office has made the restriction requirement final and so has withdrawn claims 20-32 from consideration. Applicant acknowledges the finality of this requirement and the resulting withdrawal, but continues to disagree with the restriction requirement for the reasons of record. But to simplify prosecution, Applicant has canceled these claims.

35 U.S.C. § 102 Rejection: Lau

Claims 1-5, 11-12, and 19 have been rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Lau (*Flip Chip Technologies pp.301-314)* for the reasons set forth on pages 3-4 of the Office Action. Applicant respectfully traverses this rejection.

The rejected claims contain several limitations relevant to this rejection. The first limitation is the formation of a wafer-level chip scale package. The second limitation is that the substrate contains a bond pad. And the third limitation is that a conductive particle contacts both (1) the stud bump and the bond pad or (2) the chip and the substrate.

The Office, however, has not substantiated that Lau anticipates any of these 3 claims limitations. As to the first limitation, the Office argues that Lau teaches a wafer-level chip scale package in Figure 9.17 on page 314. The legend to this Figure indicates that this is a COB assembly using a double-layer ACF. Page 301 discloses that COB stands for a "chip-on-board." The Office, however, has not shown that a chip-on-board assembly would qualify as a wafer-level chip scale package.

As to the second limitation, the Office alleges that Lau teaches a substrate with bond pads by disclosing a PCB with electrodes (the boxes on the PCB) in the device shown in Figure 9.17. Assuming that the Office is correct in this allegation (an assumption which Applicant traverses for the record), it still does not show that the PCB contains bond pads. At best, the Office has only alleged that the PCB contains electrodes. But the Office has not shown that the skilled artisan would have considered the "boxes" on the PCB in the device depicted in Figure 9.17 as bond pads.

As to the third limitation, the Office again argues that such a limitation is again described in the device of Figure 9.17. Lau discloses that this device contains a double-layer ACF layer consisting of non-filled layer and another layer filled with conducting particles that was used where very fine interconnections were needed. *See page 313.* As illustrated in Figure 9.17, the dual-layer ACF therefore consists of an upper "non-filled" adhesive layer and a lower adhesive layer "filled" with conductive particles. Thus, the skilled artisan would have recognized that the device in Figure 9.17 does not disclose a conductive particle that contacts both (1) the stud bump and the bond pad or (2) the chip and the substrate.

The Office, therefore, has not substantiated that Lau anticipates every limitation in the rejected claims. Consequently, Applicant respectfully requests withdrawal of this ground of rejection.

35 U.S.C. § 103 Rejection: Lau

Claims 6-10 and 13-18 have been rejected under 35 U.S.C. § 103 as being unpatentable over Lau for the reasons set forth on pages 5-8 of the Office Action. Applicant respectfully traverses this rejection.

The Office acknowledges that the rejected dependent claims contain limitations that are not taught by Lau. The Office alleges for various reasons that such limitations would have been obvious to the skilled artisan in light of the disclosure of Lau. Even if such allegations were true (an assumption that Application traverses for the record), such allegations do not show how the three claims limitations discussed above would have been obvious to the skilled artisan.

Thus, the Office has not substantiated that the rejected claims would have been obvious to the skilled artisan in light of Lau. Accordingly, Applicant respectfully requests withdrawal of this ground of rejection.

35 U.S.C. § 102 Rejection: Otsuka

Claims 1-7, 11-13, 15-16, and 18-19 have been rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Otsuka (U.S. Patent No. 5,949,142) for the reasons set forth on pages 8-10 of the Office Action. Applicant respectfully traverses this rejection.

The rejected claims contain several limitations pertinent to this rejection. The first limitation is the formation of a wafer-level chip scale package. The second limitation is that the substrate contains a bond pad. And the third limitation is that the claimed packaged device (or package) does not contain any solder paste.

The Office, however, has not substantiated that Otsuka anticipates any of these 3 claims limitations. As to the first limitation, the Office argues that Lau teaches a wafer-level chip scale package in the device depicted in Figure 3 and its accompanying description in column 4. As noted in several places throughout Ostuka, the devices—including that depicted in Figure 3—are "chip scale packages." *See column 3, line 60; column 4, lines 51 and 65; column 5, lines 27 and*

32, etc.... The Office, however, has not shown that such a disclosure would anticipate the claimed "wafer-level" chip scale package.

As to the second limitation, the Office alleges that Otsuka teaches a conductive substrate [5] in the device of Figure 3. Notably absent from the Office's allegation is any mention that the device in Figure 3 contains any bond pads on the substrate 5. Thus, the Office has not substantiated its burden of proof to show that this limitation is taught by Otsuka.

As to the third limitation, the Office argues that such a limitation is described in the device of Figure 3 of Otsuka. In the device of Figure 3, Otsuka describes that a silver paste is formed as projections and allowed to solidify when forming the flexible board 4 of Figure 2 (which is substantially similar to flexible board 5 in Figure 5). *See column 4, lines 4-12.* In light of this express disclosure of using this paste, the Office has failed to substantiate its burden of proof of showing that this third limitation of no solder paste is anticipated by Otsuka.

The Office, therefore, has not substantiated that Otsuka anticipates every limitation in the rejected claims. Consequently, Applicant respectfully requests withdrawal of this ground of rejection.

35 U.S.C. § 103 Rejection: Otsuka

Claims 8-10, 14, and 17 have been rejected under 35 U.S.C. § 103 as being unpatentable over Lau for the reasons set forth on pages 10-12 of the Office Action. Applicant respectfully traverses this rejection.

The Office acknowledges that the rejected dependent claims contain limitations that are not taught by Otsuka. The Office alleges for various reasons that such limitations would have been obvious to the skilled artisan in light of the disclosure of Otsuka. Even if such allegations

were true (an assumption that Application traverses for the record), such allegations do not show how the three claims limitations discussed above would have been obvious to the skilled artisan.

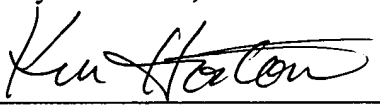
Thus, the Office has not substantiated that the rejected claims would have been obvious to the skilled artisan in light of Otsuka. Accordingly, Applicant respectfully requests withdrawal of this ground of rejection.

CONCLUSION

For the above reasons, Applicant respectfully requests the Office to withdraw the pending grounds of rejection and allow all the pending claims.

If there is any fee due in connection with the filing of this Amendment, including a fee for any extension of time not accounted for above, please charge the fee to our Deposit Account No. 50-0843.

Respectfully Submitted,

By 

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